

LogiCAN: Adaptable CAN Core IP

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Outlining the Need

When looking at various CAN applications, an extreme set of such are in complete contrary to the mass-automotive scale. Many CAN usages are in rather small quantities. In such a category various defense systems find their classifications.

When considering defense CAN design, some aspects remain almost as in mass-quantity scale (such as: reliability, upgradeability). However, few are of premium concern. Driven from the very small quantities scale (in the hundreds to thousands), defense CAN designs often rely on an easily modifiable hardware – FPGA components.

Furthermore, niche defense needs put some varying requirements over CAN controllers and logic that are hard to find in the common CAN controller chips (standalone for sure, but also in the CPU - embedded CAN peripherals). One example of importance here is the implementation of redundancy (deployment of 2 or even 3 CAN media-hardware for the purpose of a single-redundant CAN network).

Last but not least, defense designs do not put a great emphasis on hardware components cost. Thus, FPGA are very welcome there, with an abundance of headroom, providing feasibility to the previously mentioned attributes.

Where do we stand here?

number of defense equipment need CAN connectivity. To cater the varying needs, we have developed a highly versatile, easily adaptable CAN controller IP.

LogiCAN has a long history of CAN involvement. In recent years, the Israeli defense industry gradually gets an increasing foothold of the global technology trade. As a result, increasing

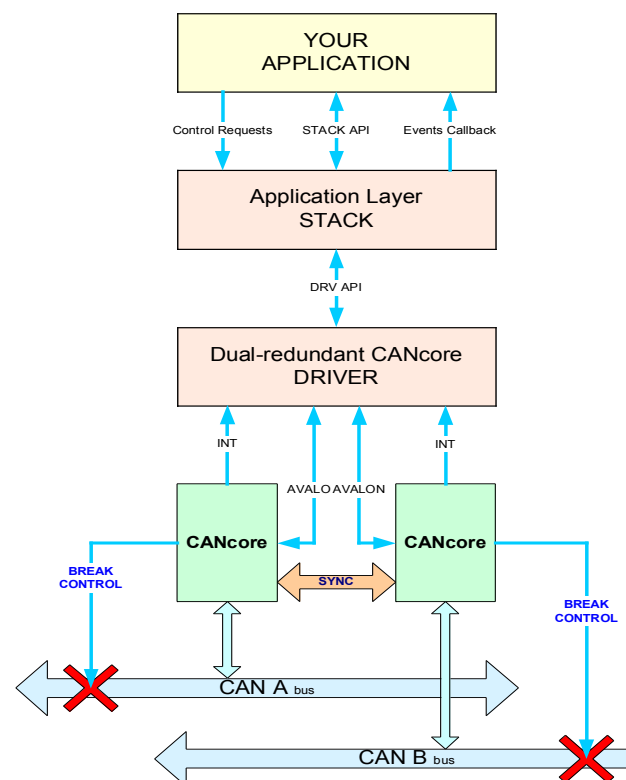
What is in the CAN controller IP?

Our CAN core is based on a basic CAN state-machine (licensed from iniCORE).

A typical core-firmware-application relationship may look as follows:

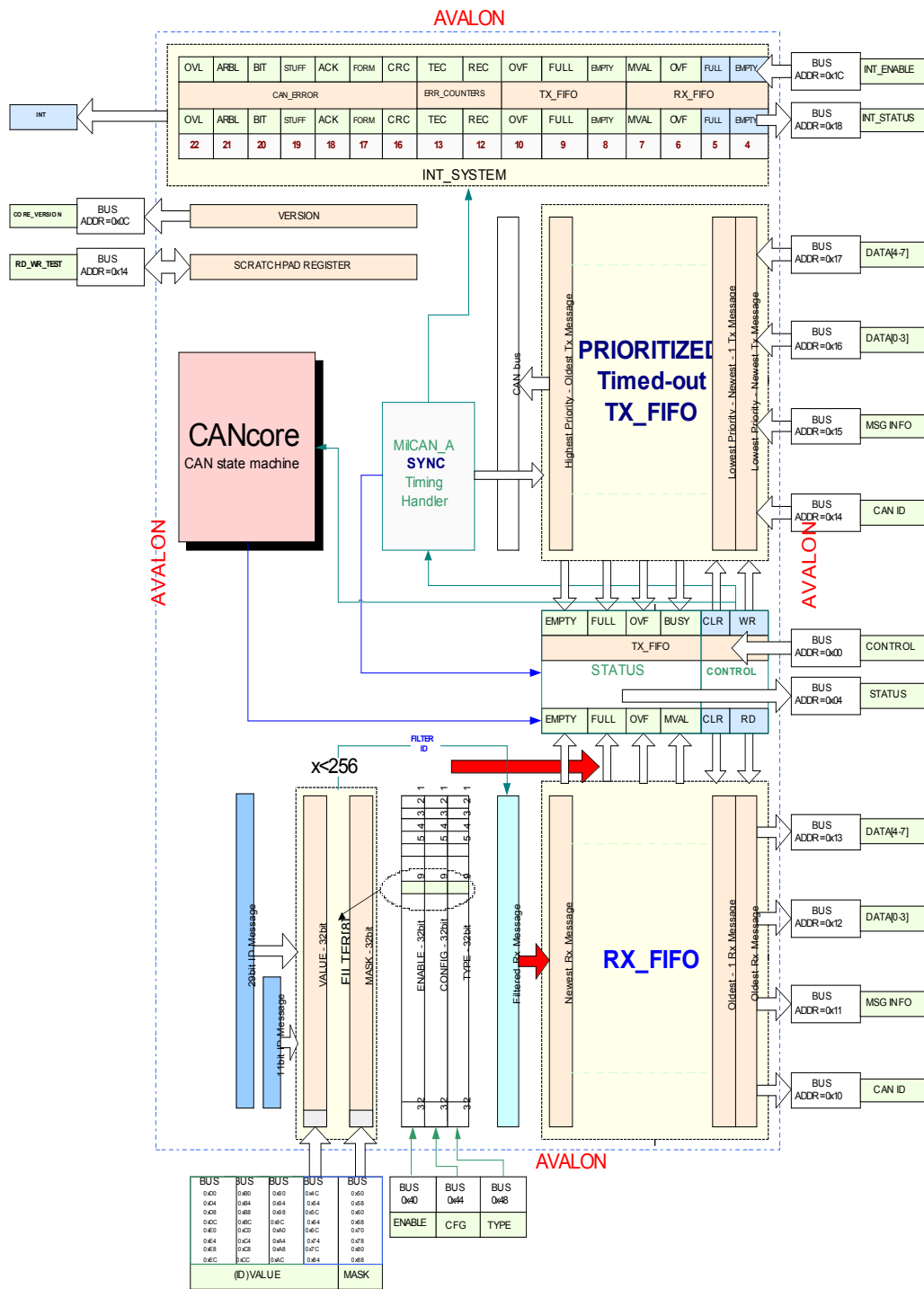
The CAN core IP main features list:

1. Flexible Interface:
ALTERA Avalon 16/32bit interface
(other buses upon request)
2. Supports all major application layers (CANopen, J1939, DeviceNet, MilCAN_A/B, SatCAN....)
3. Adaptable Resources:
 - a. Variable depth (2 to 255) RX message FIFO
 - b. Variable depth (2 to 255) TX message FIFO



7. 16bit internal **time-stamp** value can be added to the first 2 data bytes of TX messages, the time point is SOF
 8. Time-stamp counter SYNC supports synchronization among multiple core instances
 9. Automatic CAN **retransmission** feature is controllable between 0 (no retransmission), 1 – 254 retransmissions and infinite (Native CAN) retransmission
 10. CAN bus **Faults** Detection and System **Revival**:
 - a. **Detect** hardware line faults (various shorts and tear)
 - b. **Detect** bus stuck-at-dominant
 - c. **Detect** baudrate mismatch
 - d. **Operate**: Provide stub disconnection control (over external relay)
 11. **Redundancy** support:
 - a. Supports dual-redundant NMEA2000 scheme
 - b. Adds proprietary coverage scheme for very long skewed redundant message detection and automatic "better" bus selection
 12. Programmable INT line activation upon any combination of all possible internal events
 13. Loopback diagnostic option
Small footprint of as low as 2400 LE per CAN unit
4. Efficient RX message filtering:
 - a. Up to 255 RX message filters (11 or 29bit ID)
 - b. First 8 filters incorporate 32bit ID MASK
 - c. Each filter can be programmed/enabled on-the-fly
 - d. RX messages include PASS filter ID for fast and easy decoding
 5. **MilCAN** support:
 - a. Independent **MilCAN_A** SYNC message detection and automatic CFG and OPR modes announcement
 - b. Independent **MilCAN_A** SYNC message Master Generator and automatic competing SYNC Masters detection and mastership grant system
 - c. TX message FIFO supports **MilCAN_A** 8-level priority message transmission scheme:
 - i. Highest priority messages transmitted first
 - ii. Within identical priority, FIFO order is maintained
 - d. TX Messages **Relevance** control:
 - i. If enabled, any timed-out message is discarded
 - ii. Using in-message 8bit timeout counter
 6. 16bit internal **time-stamp** value is added to each RX message, the time point is SOF

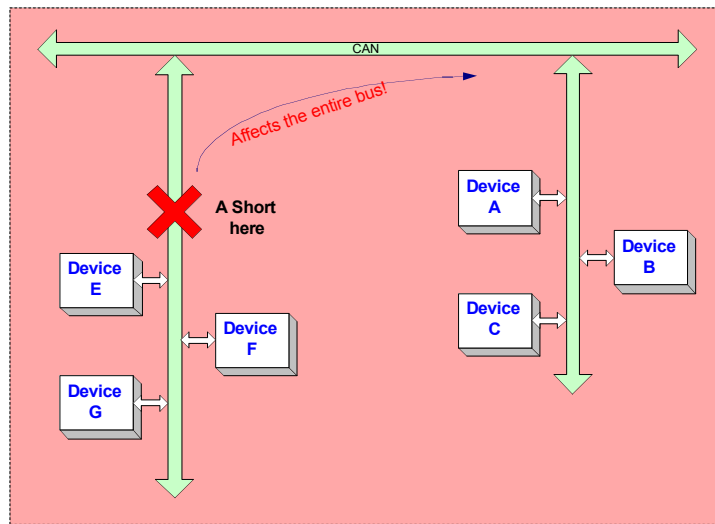
The inside of LogiCAN's CAN IP core:



Mission-Critical Support:

In an overall network, the CANfuse operation is shown in the following picture:
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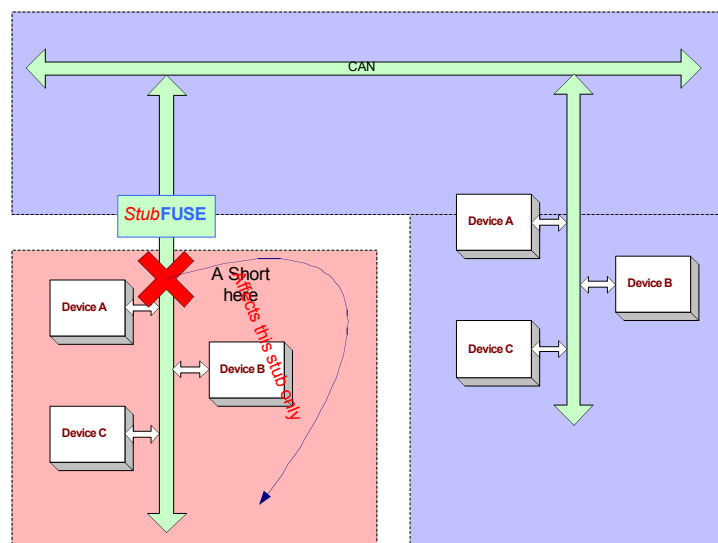
As an optional part of our CAN CORE IP, we deliver some proven support for mission-critical applications. One of these add-ons is named: CANfuse. This section describes this feature in further details.



The trunk side (left side of the picture) is protected against shorts and disturbances that may originate in the stub side (Lower left side of the picture, Devices E, F and G

not shorted, will release the relay back to normal operation

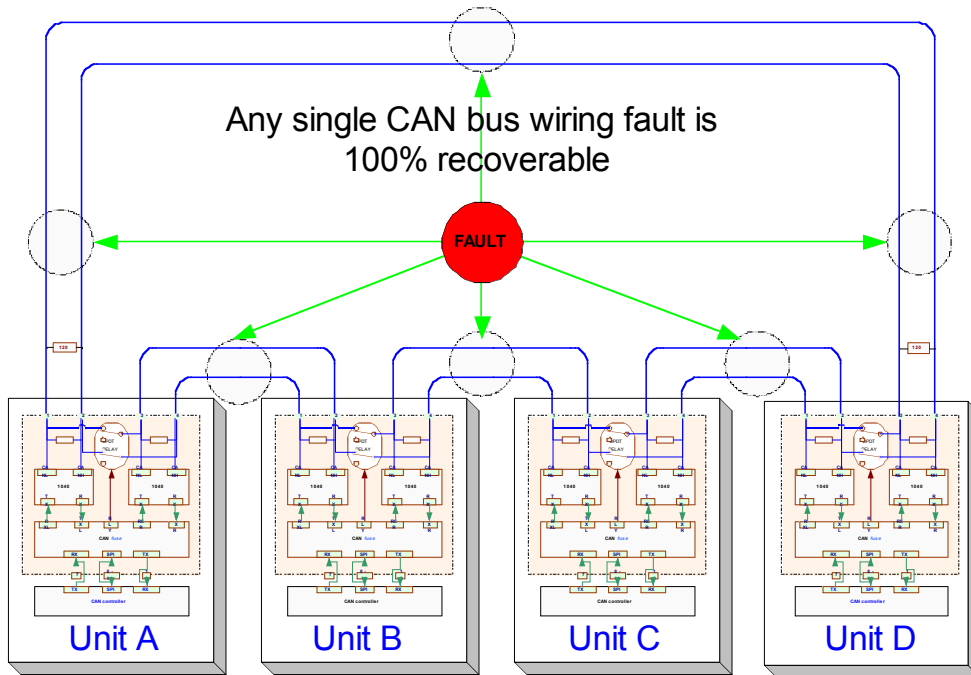
If a short occurs in the network, all **CANfuse** will trip their relays. However, within a pre-defined timeout period, all those who's stub is



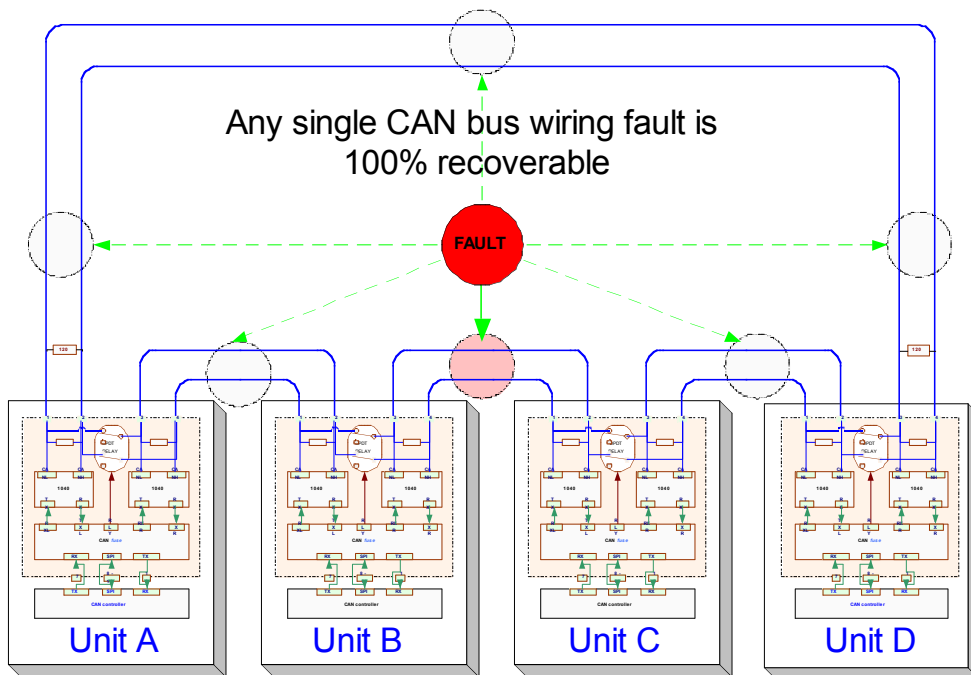
Fault Confinement

The drawings below show cases of faults and the resultant system integrity:

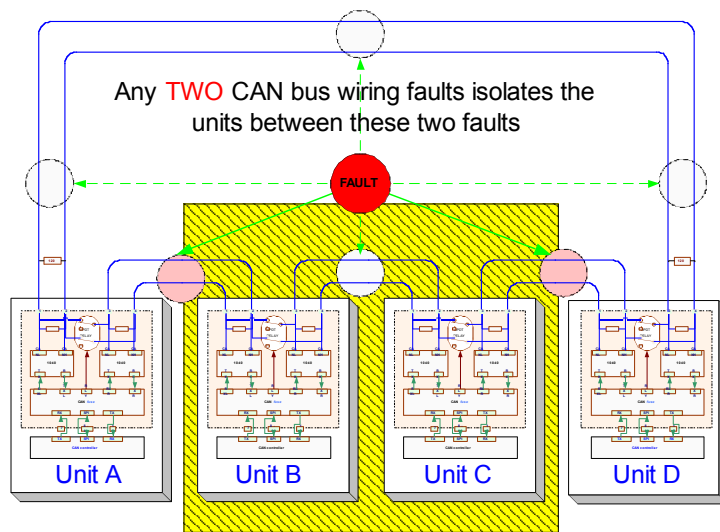
Locations of potential fault



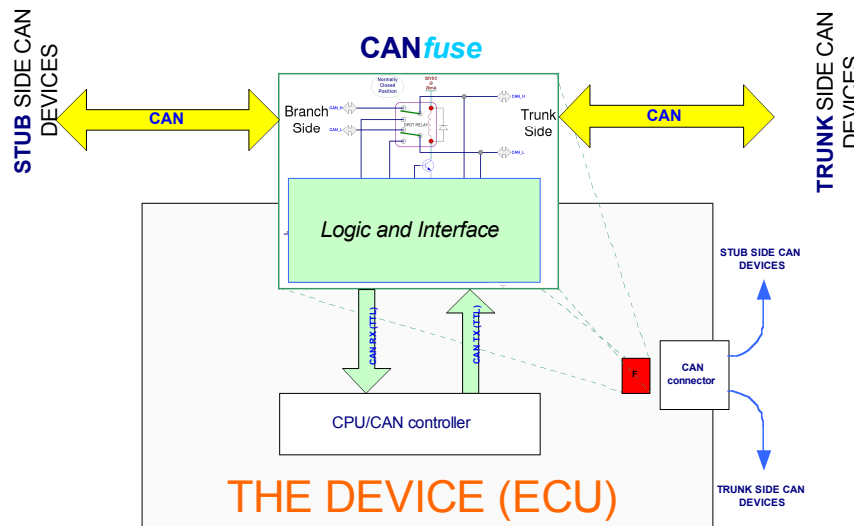
A case of a single fault



A case of double fault



Hookup details



applications, the core offers highest reliability of redundant and single CAN solutions for mission-critical needs in small to medium quantity production size.

Summary:

The presented CAN core IP design results from 8+ years of active involvement in applying FPGA-based CAN solutions to various customers in diverse applications. Already used in Israel's space program, defense equipment and many industrial

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